

IN THE CLAIMS

1. A circuit for regulating the output power of a power amplifier during a switching transient comprising:

a detector circuit coupled to a regulator and to a control signal that is generated to control the output power of the power amplifier, wherein the detector circuit detects switching transients of the power amplifier; and
a circuit coupled to the regulator for applying a signal to decrease the settling time of the regulator during a detected switching transient.

2. The circuit of claim 1, further comprising a timer circuit coupled to the bias circuit and the detector circuit for controlling when the signal is applied to the regulator.

3. The circuit of claim 2, wherein the timer is a pulse generator.

4. The circuit of claim 2, wherein the timer is a 1-shot timer.

5. The circuit of claim 1, wherein the detector detects when the voltage level of the voltage control signal drops.

6. The circuit of claim 1, wherein the detector is comprised of a slew detector.

7. The circuit of claim 1, wherein the circuit decreases the settling time of the regulator by applying a bias current to the regulator.

8. The circuit of claim 1, wherein the circuit decreases the settling time of the regulator by applying a bias voltage to the regulator.
9. The circuit of claim 1, further comprising a second regulator, wherein the circuit decreases the settling time of the regulator by selectively using the first and second regulators.
10. The circuit of claim 1, further comprising a switching device coupled to the detector, wherein the circuit decreases the settling time of the regulator by turning on the switching device in response to a detected condition.
11. The circuit of claim 10, wherein the switching device is coupled to a bias circuit and the regulator for biasing the regulator while the switching device is turned on.
12. A circuit for regulating the output power of a power amplifier during a switching transient comprising:
a regulator;
a detector for detecting a condition relating to the operation of the regulator; and
control circuitry coupled to the regulator for decreasing the settling time of regulator in response to a detected condition.
13. The circuit of claim 12, further comprising a timer coupled to the detector and the control circuitry for controlling the duration that the control circuitry controls the output power of the regulator in response to a detected condition.

14. The circuit of claim 13, further comprising delay circuitry for delaying when the control circuitry controls the output power of the regulator in response to a detected condition.
15. The circuit of claim 12, wherein the output level of the regulator is controlled by a power control signal, and wherein the detector detects a condition relating to the power control signal.
16. The circuit of claim 15, wherein the detector detects when the power control signal level drops.
17. The circuit of claim 12, wherein the control circuitry varies the speed at which the regulator is able to respond to a detected condition.
18. The circuit of claim 17, wherein the regulator is dynamically biased in response to a detected condition.
19. The circuit of claim 12, wherein the control circuitry varies the method by which the regulator controls the output power of the power amplifier in response to a detected condition.
20. The circuit of claim 19, further comprising switching circuitry for selectively activating two or more regulators in response to a detected condition.

Claims 21-48 (canceled)